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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,276	01/14/2002	Goro Nakatani	040894-5755	4701

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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,276	NAKATANI ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *5-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6410414) in view of Toyosawa et al. (US 6441467), hereinafter Toyosawa.

Regarding claim 1, Fig. 6 of Lee shows semiconductor device comprising:

a first interconnect layer (102) arranged above a substrate (100) on which a functional semiconductor region is formed (col. 3, lines 7-10);

an inter layer dielectric (104) covering a surface of the first interconnect layer;

a silicon nitride film (106; col.3, line 28) formed so as to cover entirely a top surface of said interlayer dielectric,

a metal interconnect layer (110) covering over said silicon nitride film; and

a planarized dielectric (116) formed on the metal interconnect layer.

Lee shows substantially the entire claimed structure except the uppermost metal layer made of gold. Fig. 1 of Toyosawa shows a gold uppermost metal layer (17; col.7, line 53) formed on the aluminum interconnection layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Toyosawa to the top metal layer of Lee since a uppermost layer made of gold increases the conductivity and mechanical strength of the interconnection layer.

Regarding claim 2, Fig. 6 of Lee shows a planarized top dielectric (116) is consisted of polyimide (col. 5, lines 47-52).

Regarding claim 3, Toyosawa discloses the silicon nitride film is formed by plasma CVD method (col. 9, lines 55-58).

In addition, "high-density plasma CVD" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 4, Fig. 6 of Lee shows a part of the polyimide layer is removed, forming a bond pad region (118) for bond wire connection through solder ball (114).

Regarding claim 8, Fig. 6 of Lee shows a semiconductor device comprising:

a first interconnect layer (102) covering a first portion of a surface of a functional semiconductor region (col. 3, lines 7-10);

an inter layer dielectric (104) covering a second portion of the surface of the functional semiconductor region and a portion of a surface of said first interconnect layer, thereby forming a contacting hole on the surface of the first interconnect layer;

a silicon nitride film (106) covering a top surface of said inter layer dielectric around the contacting hole on the surface of the first interconnect layer;

a metal interconnect region (110); and

a planarized dielectric (116) covering the metal interconnect layer and the silicon nitride surface around the metal interconnect region.

Lee fails to show a barrier layer formed around the contact hole for the gold metal layer. Fig. 1 of Toyosawa shows a barrier metal layer (16; col.7, lines 48-51) formed around the contact hole for the gold metal layer (17).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Toyosawa to the device of Lee in order to have a barrier metal layer around the contact hole since the barrier layer provides a better adhesion of the metal layer to the dielectric layer which aspect is well known in the art. And It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Toyosawa to the top metal layer of Lee since a uppermost layer made of gold increases the conductivity and mechanical strength of the interconnection layer.

Regarding claim 9, Toyosawa disclose that the barrier layer consists of titanium (col. 7, lines 48-50).

Regarding claims 10 and 11, Lee discloses the first interconnect layer consists of aluminum (col. 3, line15).

Regarding claim 12, Lee discloses the inter layer dielectric consists of USG film (siliconoxide; col.3, lines 28-29).

Regarding claim 13, Fig. 1 of Toyosawa shows the functional semiconductor region further comprises a polysilicon gate (3) isolated from the first interconnect layer by a second dielectric layer (10), wherein the first interconnect layer is connected to the polysilicon gate through a contacting area disposed within the second dielectric layer.

Response to Arguments

Applicant's arguments filed January 29, 2004 have been fully considered but they are not persuasive.

First, Applicant argues that "Toyosawa merely discloses forming gold-bump to protect electrode pads" while the instant invention recites "an upper metal interconnect layer is formed with gold." However, Figure 1 of Toyosawa shows that the gold bump (17) is formed as an uppermost metal layer and the top surface (30) of the gold bump is an electrode pad (for connection to a conductive element). Therefore, the claimed limitation of "an upper metal interconnect layer is formed with gold" is readable on the gold bump of Toyosawa.

Applicant further contends that "Toyosawa is not analogous to the interconnect layer of the instant invention because of their technical differences and distinct functionalities." Examiner would like to point out that technically distinct functionalities are not recited in the pending claim. In addition, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. *In re Danly*, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does."(emphasis in original) Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Second, Applicant argues that the instant invention recites "planarization is performed using a dielectric material" in contrast to "the planarization of Toyosawa is performed by SOG." Note that SOG is performed using a dielectric material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800